CLAIMS

What is claimed is:

1. A method of fabricating an integrated circuit package comprising:

providing a semiconductor die having a plurality of bond pads on an active surface thereof;

providing a lead frame including a plurality of conductive leads;

electrically coupling a first bond pad of the plurality of bond pads to a first portion of at least one conductive lead;

electrically coupling a second bond pad of the plurality of bond pads to a second portion of the at least one conductive lead; and

electrically isolating the first portion of the at least one conductive lead from the second portion of the at least one conductive lead.

2. The method of claim 1, further comprising encapsulating the semiconductor die and at least a portion of the lead frame in a dielectric material.

3. The method of claim 2, wherein the electrically isolating the first portion from the second portion is effected subsequent to the encapsulating.

4. The method of claim 1, wherein the electrically isolating the first portion from the second portion of the at least one conductive lead includes mechanically severing the at least one conductive lead between the first portion and the second portion.

5. The method of claim 1, wherein the electrically isolating the first portion from the second portion of the at least one conductive lead includes etching to sever the at least one conductive lead between the first portion and the second portion.

6. The method of claim 1, wherein the electrically coupling the first bond pad to a first portion of the at least one conductive lead includes wire bonding.

7. The method of claim 6, wherein electrically coupling the second bond pad to a second portion of the at least one conductive lead includes wire bonding.

8. The method of claim 1, further comprising forming a notched region in a surface of the at least one conductive lead between the first portion and the second portion.

9. The method of claim 8, further comprising encapsulating the semiconductor die and at least a portion of the lead frame including the notched region of the at least one conductive lead in a dielectric material.

10. The method of claim 9, wherein the electrically isolating the first portion from the second portion includes separating the first portion from the second portion while leaving at least some dielectric material in the notched region.

11. The method of claim 10, wherein the separating the first portion from the second portion includes cutting the at least one conductive lead into the notched region from an opposing surface of the at least one conductive lead.

12. A method of forming an array of electrically conductive elements on an integrated circuit package, the method comprising:

securing a semiconductor die having a plurality of bond pads on an active surface thereof to a lead frame having a plurality of leads;

electrically coupling each lead of the plurality of leads at spaced locations with one of at least two different bond pads of the plurality of bond pads; and

severing each lead between the spaced locations to form at least two electrically isolated conductive elements.

13. A lead frame comprising:

a plurality of leads, including at least one lead having:

a first bonding region,

a second bonding region, and

a severance region located between the first bonding region and the second bonding region, the severance region being configured to facilitate separation of the first bonding region from the second bonding region.

14. The lead frame of claim 13, wherein the severance region includes a notch in the lead.

15. The lead frame of claim 13, wherein each of the plurality of leads include a first bonding region, a second bonding region, and a severance region configured to facilitate separation of the first and second bonding regions.

16. The lead frame of claim 15, wherein each severance region includes a notch.

17. A lead frame for an integrated circuit package, the lead frame comprising:

a die paddle configured for attachment to a semiconductor die; and

a plurality of conductive elements each having at least two bonding regions arranged in a grid array about the die paddle, the grid array including at a first peripheral row of bonding regions spaced about a periphery of the die paddle and at least one other peripheral row of bonding regions spaced outwardly from the first peripheral row of bonding regions.

18. An integrated circuit package comprising:

a semiconductor die;

a plurality of conductive elements arranged in an array, the array including at least a first set of spaced and electrically isolated conductive elements adjacent an outer lateral periphery of the integrated circuit package and at least one other set of spaced and electrically isolated conductive elements inwardly adjacent the first set, the at least two sets of conductive elements being located outside a lateral periphery of the semiconductor die;

an dielectric encapsulant formed over the semiconductor die and defining the outer lateral periphery of the integrated circuit package, the dielectric encapsulant extending at least partially laterally about the conductive elements and leaving an outer surface of each conductive element exposed; and

a recess in the encapsulant material between at least one conductive element of the first set of conductive elements and at least one adjacent conductive element of the at least one other set of conductive elements.

19. The integrated circuit package of claim 18, wherein the semiconductor die includes a plurality of bond pads and wherein each of the plurality of bond pads are electrically connected with a conductive element of the plurality of conductive elements.

20. The integrated circuit package of claim 19, wherein the electrical connection between each of the plurality of bond pads and each respective conductive element of the plurality of conductive elements includes a wire bond.

21. The integrated circuit package of claim 18, wherein the conductive elements of the first set of conductive elements are substantially aligned with the conductive elements of the at one other set transverse to an adjacent outer lateral peripheral edge of the integrated circuit package.

22. The integrated circuit package of claim 21, wherein the conductive elements of the first set of conductive elements are offset relative to the conductive elements of the at one other set.

23. The integrated circuit package of claim 18, wherein the recess comprises an elongated, trough-like recess extending substantially between conductive elements of the first set and conductive elements of the second set disposed along a common laterally outer peripheral edge of the integrated circuit package.

24. A semiconductor die assembly, comprising:

a semiconductor die having a plurality of bond pads;

a lead frame having a plurality of conductive leads, each lead being electrically coupled at spaced locations on the lead to at least two bond pads of the plurality of bond pads.

25. The integrated circuit package of claim 24, further comprising a dielectric encapsulant formed about the semiconductor die and partially about the lead frame.

26. The integrated circuit package of claim 24, further comprising a wire bond coupling each lead at the spaced locations thereon to one of the at least two bond pads of the plurality of bond pads.

27. The integrated circuit package of claim 26, wherein each lead includes a severance region configured to facilitate separation into at least two mutually electrically isolated conductive elements.

28. A memory module comprising:

a module board configured to be electrically coupled with a higher level of packaging; and

at least one integrated circuit package electrically coupled with the module board, the integrated circuit package comprising:

a semiconductor die;

a plurality of conductive elements arranged in an array, the array including at least a first set of spaced and electrically isolated conductive elements adjacent an outer lateral periphery of the integrated circuit package and at least one other set of spaced and electrically isolated conductive elements inwardly adjacent the first set, the at least two sets of conductive elements being located outside a lateral periphery of the semiconductor die;

an dielectric encapsulant formed over the semiconductor die and defining the outer lateral periphery of the integrated circuit package, the dielectric encapsulant extending at

least partially laterally about the conductive elements and leaving an outer surface of each conductive element exposed; and

a recess in the encapsulant material between at least one conductive element of the first set of conductive elements and at least one adjacent conductive element of the at least one other set of conductive elements.

29. A computer system comprising:

an input device;

an output device;

a processor coupled to the input and output devices; and

a memory module coupled to the processor, the memory module comprising a module board coupled to at least one integrated circuit package comprising:

a semiconductor die;

a plurality of conductive elements arranged in an array, the array including at least a first set of spaced and electrically isolated conductive elements adjacent an outer lateral periphery of the integrated circuit package and at least one other set of spaced and electrically isolated conductive elements inwardly adjacent the first set, the at least two sets of conductive elements being located outside a lateral periphery of the semiconductor die;

an dielectric encapsulant formed over the semiconductor die and defining the outer lateral periphery of the integrated circuit package, the dielectric encapsulant extending at least partially laterally about the conductive elements and leaving an outer surface of each conductive element exposed; and

a recess in the encapsulant material between at least one conductive element of the first set of conductive elements and at least one adjacent conductive element of the at least one other set of conductive elements.

30. A semiconductor die assembly, comprising:

a semiconductor die having a plurality of bond pads on an active surface thereof;

at least one set of mutually spaced conductive elements laterally outboard of at least one peripheral edge of the semiconductor die, and at least another set of mutually spaced conductive elements spaced from and laterally outboard of the at least one set of conductive elements;

a plurality of wire bonds extending between bond pads of the plurality and conductive elements of the first and second sets; and

a package comprising dielectric material extending over the semiconductor die and wire bonds and having an outer lateral periphery substantially coincident with outer lateral extents of the at least one other set of conductive elements, dielectric material of the package extending at least partially about each of the conductive elements and leaving a surface thereof exposed.

31. The semiconductor die assembly of claim 30, further comprising a die paddle to which the semiconductor die is secured by a back side thereof.

32. The semiconductor die assembly of claim 30, wherein the at least one set of mutually spaced conductive elements and the at least another set of conductive elements extend around a plurality of peripheral edges of the semiconductor die.

33. The semiconductor die assembly of claim 30, wherein the at least one set of mutually spaced conductive elements and the at least another set of conductive elements extend around four peripheral edges of the semiconductor die.

34. The semiconductor die assembly of claim 30, further including an elongated, trough-like recess extending between conductive elements of the at least one set and conductive elements of the at least another set and substantially parallel to the at least one peripheral edge of the semiconductor die.

35. The semiconductor die assembly of claim 30, wherein the exposed surfaces of the

conductive elements are oriented substantially parallel to the active surface of the semiconductor die.

36. A method of fabricating a semiconductor die assembly, comprising:

placing a semiconductor die within a plurality of leads extending laterally outwardly from peripheral edges thereof;

wire bonding bond pads on the semiconductor die to spaced locations on the leads of the plurality;

transfer molding a dielectric encapsulant over the semiconductor die, wire bonds and leads, leaving undersurfaces of the leads exposed; and

severing the leads between the spaced locations.

37. The method of claim 36, further comprising notching upper surfaces of the leads between the spaced locations before the placing the semiconductor die within the plurality of leads.

38. The method of claim 36, wherein the placing the semiconductor die includes securing the semiconductor die to a die paddle located within the plurality of leads.

39. The method of claim 36, wherein the severing is effected by making a linear cut between the spaced locations on each lead extending from a common peripheral edge.

40. The method of claim 39, further comprising notching upper surfaces of the leads between the spaced locations before the placing the semiconductor die within the plurality of leads, and wherein the linear cut is extended substantially only to a depth sufficient to intersect bottoms of the notches so that some dielectric material remains between the spaced locations.

41. A lead frame strip, comprising:

a plurality of longitudinally arranged lead frames, each lead frame including an outer frame portion bearing a plurality of inwardly extending, cantilevered leads, and each lead of the plurality

having thereon at least two longitudinally spaced locations separated by a severance region comprising a notch extending laterally across the lead.

42. The lead frame strip of claim 41, wherein each outer frame portion further bears a die paddle substantially centered therein.

43. The lead frame strip of claim 41, wherein the plurality of inwardly extending, cantilevered leads are located on a plurality of sides of each outer frame portion.

44. The lead frame strip of claim 41, wherein the plurality of inwardly extending, cantilevered leads are located on four sides of each outer frame portion.